REMARKS/ARGUMENT

Objected to Claims 8, 11, 16 and 19 have been amended to overcome the informalities identified by Examiner.

1) Claims 1, 4, 6, 9, 10, 14, 17, 18 and 21 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ahn et al. (U.S. Publication No. 2002/0080891). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1, 4, 6, 9, 10, 14, 17, 18 and 21 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California,* 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.,* 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, an integrated transceiver circuit, comprising: "a **digital polar transmitter path that provides an amplitude/phase signal from a digital input**, the transmitter path including at least one digital predistorter that predistorts the digital input to mitigate nonlinearities associated with a power amplifier", "a receiver path associated with the digital transmitter path", "a coupling element that provides the signal from the transmitter path to the receiver path" and "a signal evaluator that determines values for at least one parameter associated with the digital predistorter based on the signal".

In contrast, Ahn teaches only Cartesian (I/Q) transmitters. Ahn fails to teach or suggest, "a **digital polar transmitter path ...**". Ahn further fails to teach or suggest, "... **that provides an amplitude/phase signal from a digital input**", as required by Claim 1. Accordingly, the 35 U.S.C. 102(e) rejection of Claim 1 is overcome.

Claims 4, 6, 9, 10, 14, 17 and 18 stand allowable as depending directly, or indirectly, respectively from allowable Claim 1.

Claim 4 further defines the circuit of claim 1, the power amplifier comprising an internal power amplifier that is integrated into the integrated transceiver circuit, **the power amplifier accepting digital RF input**. Claim 4 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Moreover, there is no teaching in Ahn that its power amplifier "accepts digital RF input". Accordingly, the 35 U.S.C. 102(c) rejection is overcome.

Claim 6 further defines the circuit of claim 4, the digital transmitter path comprising an **amplitude modulated path** that provides a supply to the internal power amplifier from a first digital input, and **a phase modulated path** that provides a radio frequency input to the internal power amplifier from a second digital input. Claim 6 depends from Claim 4 and stands allowable for the same reasons set forth above in support of the allowability of Claim 4. Moreover, Ahn does not teach or suggest "the digital transmitter path comprising an amplitude modulated path" or "and a phase modulated path", as required by Claim 6. The text cited by the Examiner "the predistorter 10 receives an RF input signal IN, changes an amplitude and phase of the received RF input signal IN" ([0007], lines 3-8), merely abstractly deals with the function of changing amplitude and phase of a received RF signal. Further it does not teach an "amplitude modulated path that provides a supply to the internal power amplifier", which operates in baseband and not RF. Similarly, it does not teach "a phase modulated path that provides a radio frequency input to the internal power amplifier". Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

Claim 9 further defines the circuit of claim 6, **the phase modulated path comprising a digital predistorter** that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier. Claim 9 depends from Claim 6 and stands allowable for the same reasons set forth above in support of the allowability of Claim 6. Moreover, Ahn does not teach or even suggest "the phase modulated path comprising a digital predistorter". The text cited by the examiner does not even mention the phase modulated path or digital predistorter. Further, Ahn does not teach or suggest the "digital predistorter that adjusts the second digital input". The cited text does not even mention the second digital input. Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

Claim 10 further defines the circuit of claim 6, **the amplitude modulated path comprising a digital predistorter** that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier. Claim 10 depends from Claim 6 and stands allowable for the same reasons set forth above in support of the allowability of Claim 6. Moreover, Ahn does not teach or suggest "the amplitude modulated path comprising a digital predistorter". The text cited by the examiner does not even mention the amplitude modulated path or digital predistorter. Further, Ahn does not teach or suggest the "digital predistorter that adjusts the first digital input". The cited text does not even mention the first digital input. Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

Claim 14 further defines the circuit of claim 12, the digital transmitter path comprising an **amplitude modulated path** that controls the supply to the external amplifier according to a first digital input, and a **phase modulated path** that provides a radio frequency input to the external power amplifier according to a second digital input. Claim 14 depends from Claim 12 and stands allowable for the same reasons set forth above in support of the allowability of Claim 12. Moreover, Ahn does not teach or suggest "the digital transmitter path comprising an amplitude modulated path" or "and a phase modulated path", as required by Claim 14. The text cited by the Examiner "the predistorter 10 receives an RF input signal IN, changes an amplitude and

phase of the received RF input signal IN" ([0007], lines 3-8), merely abstractly deals with the function of changing amplitude and phase of a received RF signal. Further it does not teach an "amplitude modulated path that provides a supply to the internal power amplifier", which operates in baseband and not RF. Similarly, it does not teach "a phase modulated path that provides a radio frequency input to the internal power amplifier". Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

Claim 17 further defines the circuit of claim 14, the phase modulated path comprising a digital predistorter that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier. Claim 17 depends from Claim 14 and stands allowable for the same reasons set forth above in support of the allowability of Claim 14. Moreover, Ahn does not teach or even suggest "the phase modulated path comprising a digital predistorter". The text cited by the examiner does not even mention the phase modulated path or digital predistorter. Further, Ahn does not teach or suggest the "digital predistorter that adjusts the second digital input". The cited text does not even mention the second digital input. Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

Claim 18 further defines the circuit of claim 14, **the amplitude modulated path comprising a digital predistorter** that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier. Claim 18 depends from Claim 14 and stands allowable for the same reasons set forth above in support of the allowability of Claim 14. Moreover, Ahn does not teach or suggest "the amplitude modulated path comprising a digital predistorter". The text cited by the examiner does not even mention the amplitude modulated path or digital predistorter. Further, Ahn does not teach or suggest the "digital predistorter that adjusts the first digital input". The cited text does not even mention the first digital input. Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

Independent Claim 21, as amended, requires and positively recites, a method of calibrating a predistortion component in a transceiver system, comprising: "**providing a first**

digital signal, containing amplitude information related to a desired analog signal, to a transmitter path", "**providing a second digital signal, containing phase information** related to the desired analog signal, to the transmitter path", "**predistorting** at least one of **the first digital signal and the second digital signal** in the digital domain according to at least one predistortion parameter", "generating an analog signal from the first digital signal and the second digital signal" and "processing the analog signal at a receiver path associated with the transmitter path to determine values for the at least one predistortion parameter".

Ahn, in contrast, does not teach "providing a first digital signal, containing amplitude information" nor "providing a second digital signal, containing phase information". The text cited by the examiner "the predistorter 10 receives an RF input signal IN, changes an amplitude and phase of the received RF input signal IN" ([0007], lines 3-8) does not even suggest, "**providing a first digital signal, containing amplitude information** related to a desired analog signal, to a transmitter path", "**providing a second digital signal, containing phase information** related to the desired analog signal, to the transmitter path", as required by Claim 21.

Further, Ahn does not teach "predistorting at least one of the first digital signal and the second digital signal in the digital domain", as required by the third element of Claim 21. The first digital signal contains amplitude information and the second digital signal contains phase information, as required by the first and second elements of Claim 21. As such, Ahn fails to teach or suggest, "**predistorting** at least one of **the first digital signal and the second digital signal** in the digital domain according to at least one predistortion parameter", as required by Claim 21. Accordingly, the 35 U.S.C. 102(e) rejection is overcome.

2) Claims 2, 3, 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claims 1, 6, and 21 above, and further in view of Park et al. (U.S. Patent No. 6,373,902). Applicants respectfully traverse this rejection,

as set forth below.

Claim 2 further defines the circuit of claim 1, in which the transmitter path comprises a **gain normalization component** that transfers the digital input **from a normalized domain** to a domain that is dependent on process, voltage, and temperature (PVT) variations. Examiner admits that Ahn fails to disclose the transmitter path comprising a gain normalization component that transfers the digital input from a normalized domain to a domain that is dependent on process, voltage, and temperature (PVT) variations. Examiner, however, relies for Park for this omitted teaching. Applicants respectfully traverse Examiner's determination for the reasons set forth below.

Ahn in view of Park does not teach "the transmitter path comprising a gain normalization component that transfers the digital input from a normalized domain to a domain that is dependent on process, voltage, and temperature (PVT) variations", as required and positively recited by Claim 2. The text cited by the examiner (Park, col. 3, lines 35-57) merely discloses a function "to update digital codes stored in a predistortion random-access-memory (RAM) 21 in a direction such as to reduce the distortion" (Park, col. 3, lines 55-57). The cited text only loosely deals with voltage compensation – NOT gain normalization. These two are different. There is no gain normalization component in Park as is conventionally understood and described in the present disclosure. For example, the "phase information associated with the normalized tuning word is normalized to an expected clock period of oscillator" (pp. 4, lines 19-20), which is not taught by Park. Further, "The IPA gain normalization component 124 operates in much the same fashion as the DCO gain normalization device. The exact gain provided by the power amplifier for a particular input is subject to process and environmental factors which cannot be known precisely, so an estimate thereof, K'_{IPA}, must be determined. The estimate K'_{IPA} can be calculated entirely in the digital domain by observing responses to past gain corrections. The actual IPA gain estimation may involve arithmetic operations, such as multiplication or division and averaging, or an exhaustive or iterative search for an optimal solution..." (pp. 10, lines 16-23). Accordingly, the estimation of the PA gain is not taught by Park. Therefore, Park fails to

teach or suggest, the circuit of claim 1, in which the transmitter path comprises a **gain normalization component** that transfers the digital input **from a normalized domain** to a domain that is dependent on process, voltage, and temperature (PVT) variations. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 3 further defines the circuit of claim 2, in which the digital predistorter precedes the gain normalization component on the transmitter path, such that the digital predistorter predistorts the digital input in the normalized domain. Claim 3 stands allowable for the same reasons set forth above in support of Claim 2. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 11 further defines the circuit of claim 6, in which the amplitude modulated path comprises a **gain normalization component** that adjusts the first digital input for process, voltage and temperature (PVT) variations associated with the internal power amplifier. Examiner admits that Ahn fails to disclose the transmitter path comprising a gain normalization component that transfers the digital input from a normalized domain to a domain that is dependent on process, voltage, and temperature (PVT) variations. Examiner, however, relies for Park for this omitted teaching. Applicants respectfully traverse Examiner's determination for the reasons set forth below.

Ahn in view of Park does not teach "the circuit of claim 6, in which the amplitude modulated path comprises a gain normalization component that adjusts the first digital input for process, voltage and temperature (PVT) variations associated with the internal power amplifier.", as required and positively recited by Claim 11. The text cited by the examiner (Park, col. 3, lines 35-57) merely discloses a function "to update digital codes stored in a predistortion random-access-memory (RAM) 21 in a direction such as to reduce the distortion" (Park, col. 3, lines 55-57). The cited text only loosely deals with voltage compensation – NOT gain normalization. These two are different. There is no gain normalization component in Park as is conventionally understood and described in the present disclosure. For example, the "phase information

associated with the normalized tuning word is normalized to an expected clock period of oscillator" (pp. 4, lines 19-20), which is not taught by Park. Further, "The IPA gain normalization component 124 operates in much the same fashion as the DCO gain normalization device. The exact gain provided by the power amplifier for a particular input is subject to process and environmental factors which cannot be known precisely, so an estimate thereof, K'_{IPA}, must be determined. The estimate K'_{IPA} can be calculated entirely in the digital domain by observing responses to past gain corrections. The actual IPA gain estimation may involve arithmetic operations, such as multiplication or division and averaging, or an exhaustive or iterative search for an optimal solution..." (pp. 10, lines 16-23). Accordingly, the estimation of the PA gain is not taught by Park. Therefore, Park fails to teach or suggest, the circuit of claim 6, in which the amplitude modulated path comprises a **gain normalization component** that adjusts the first digital input for process, voltage and temperature (PVT) variations associated with the internal power amplifier. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 22 further defines the method of claim 21, by further comprising converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains. Examiner admits that Ahn fails to disclose converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains. Examiner, however, relies for Park for this omitted teaching. Applicants respectfully traverse Examiner's determination for the reasons set forth below.

Ahn in view of Park does not teach "converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains", as required and positively recited by Claim 22. The text cited by the examiner (Park, col. 3, lines 35-57) merely discloses a function "to update digital codes stored in a predistortion random-access-memory (RAM) 21 in a direction such as to reduce the distortion" (Park, col. 3, lines 55-57). The cited text only loosely deals with voltage compensation – NOT gain normalization. These two are different. There is no gain normalization component in Park

as is conventionally understood and described in the present disclosure. For example, the "phase information associated with the normalized tuning word is normalized to an expected clock period of oscillator" (pp. 4, lines 19-20), which is not taught by Park. Further, "The IPA gain normalization component 124 operates in much the same fashion as the DCO gain normalization device. The exact gain provided by the power amplifier for a particular input is subject to process and environmental factors which cannot be known precisely, so an estimate thereof, K'_{IPA}, must be determined. The estimate K'_{IPA} can be calculated entirely in the digital domain by observing responses to past gain corrections. The actual IPA gain estimation may involve arithmetic operations, such as multiplication or division and averaging, or an exhaustive or iterative search for an optimal solution..." (pp. 10, lines 16-23). Accordingly, the estimation of the PA gain is not taught by Park. The 35 U.S.C. 103(a) rejection is overcome.

Further, the first and second digital signals of Claim 22 are amplitude and phase information, which is not taught or suggested by any combination of Ahn and Park.

To establish *a prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143).

Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill *in the* art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee*, 277 F.3d 1338, 1342-44, 61 USPQ2d

1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones, 958* F.2d *347, 21* USPQ2d 1941 (Fed. Cir. 1992).

Applicants further point out that any statement that modifications of the prior art to meet the claimed invention would have been "well within the ordinary skill of *the* art at *the* time the claimed invention was made" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish *a* prima *facie case of* obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood, 28* USPQ2d 1300 (Bd. Pat. App. & Inter. *1993).* See also *In re Kotzab,* 217 F.3d 1365, 1371, 55 USPQ2d *1313,* 1318 (Fed. Cir. 2000) (Court reversed obviousness rejection involving technologically simple concept because there was no finding as to the principle or specific understanding within the knowledge of a skilled artisan that would have motivated the skilled artisan to make the claimed invention); *Al-Site Corp. v. VSIInt'l Inc.,* 174 F.3d 1308,50 USPQ2d 1161 (Fed. Cir. 1999) (The level of skill in the art cannot be relied upon to provide the suggestion to combine references).

3) Claims 5, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claims 1, 4, and 21 above, and further in view of Kee et al. (U.S. Patent No. 6,724,255). Applicants respectfully traverse this rejection, as set forth below.

Claim 5 further defines the circuit of claim 4, the **internal power amplifier comprising a Class E switching amplifier**. Examiner admits that Ahn fails to teach or suggest that the internal power amplifier comprises a Class E switching amplifier. Examiner, however, relies upon Kee as disclosing this limitation. Applicants respectfully point out that even if, arguendo, Kee were to disclose an internal power amplifier comprising a Class E switching amplifier, Kee fail to teach or suggest the previously discussed deficiencies of the Ahn reference as discussed

above in support of the allowability of Claim 4. In addition, Applicants point out that Examiner's proposed combination of Kee and Ahn will not work. Kee's Class E switching amplifier requires digital RF clock input and will not work with amplitude modulated inputs from Ahn. For example, the power amplifier 140 in Ahn must be linear in the conventional definition of the word and requires Class A, B, AB or C of operation. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 20 further defines the circuit of claim 1, the transmitter path being operative to alternate between a saturation mode, in which the power amplifier is driven at saturation, and a linear mode, in which the power amplifier operates within a linear range. Examiner admits that Ahn fails to disclose adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation. Examiner relies upon Kee's switching amplifier for this additional teaching. Applicants respectfully point out that even if, arguendo, Kee were to disclose adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation, Kee fail to teach or suggest the previously discussed deficiencies of the Ahn reference as discussed above in support of the allowability of Claim 1.

Moreover, the capability to "alternate between a saturation mode, in which the power amplifier is driven at saturation, and a linear mode, in which the power amplifier operates within a linear range" has nothing to do with the long-lasting design decision to select either a linear-mode PA or saturated-mode PA: "the switching amplifier as disclosed by Kee in claim 5 above meets the limitations of switching from a linear to a saturated mode which he discloses has the benefit of eliminating causes of switching power dissipation (...). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to employ the Class E switching amplifier as disclosed by Kee into the invention of Ahn" (office action, pp. 6). The motivation has rather to do with multi-mode operation to handle various standards: "For example, the system could alternate between an EDGE modulation scheme and a GSM

modulation arrangement." (pp. 18, lines 9-10). Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 23 further defines the method of claim 21, further comprising adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation. Examiner admits that Ahn fails to disclose adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation. Examiner relies upon Kee's switching amplifier for this additional teaching. Applicants respectfully point out that even if, arguendo, Kee were to disclose adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation, Kee fail to teach or suggest the previously discussed deficiencies of the Ahn reference as discussed above in support of the allowability of Claim 11.

Moreover, the capability to "alternate between a saturation mode, in which the power amplifier is driven at saturation, and a linear mode, in which the power amplifier operates within a linear range" has nothing to do with the long-lasting design decision to select either a linear-mode PA or saturated-mode PA: "the switching amplifier as disclosed by Kee in claim 5 above meets the limitations of switching from a linear to a saturated mode which he discloses has the benefit of eliminating causes of switching power dissipation (...). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to employ the Class E switching amplifier as disclosed by Kee into the invention of Ahn" (office action, pp. 6). The motivation has rather to do with multi-mode operation to handle various standards: "For example, the system could alternate between an EDGE modulation scheme and a GSM modulation arrangement." (pp. 18, lines 9-10). Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

4) Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ahn et al. (U.S. Pub. No. 2002/0080891) as applied to claim 4 above, and further in view of Kim et al. (U.S. Patent No. 2002/0034260). Applicants respectfully traverse this rejection, as set forth below.

Claim 7 further defines the circuit of claim 6, the phase modulated path comprising a digitally controlled oscillator. Examiner admits that Ahn fails to disclose the phase modulated path comprising a digitally controlled oscillator (fig. 4, NCO element 47). Applicants respectfully point out that even if, arguendo, Kim were to disclose a phase modulated path comprising a digital controlled oscillator, Kim fails to teach or suggest the previously discussed deficiencies of Ahn as applied to Claim 6. Moreover, Kim does not disclose the phase modulated path comprising a digitally-controlled oscillator. NCO element 47 in Figure 4 is not part of the phase modulated path. The phase modulation does not involve NCO 47. In fact, NCO 47 does not have shown any modulating input. The principle of operation there is entirely different. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 15 further defines the circuit of claim 14, the phase modulated path comprising a digitally controlled oscillator. Examiner admits that Ahn fails to disclose the phase modulated path comprising a digitally controlled oscillator (fig. 4, NCO element 47). Applicants respectfully point out that even if, arguendo, Kim were to disclose a phase modulated path comprising a digital controlled oscillator, Kim fails to teach or suggest the previously discussed deficiencies of Ahn as applied to Claim 14. Moreover, Kim does not disclose the phase modulated path comprising a digitally-controlled oscillator. NCO element 47 in Figure 4 is not part of the phase modulated path. The phase modulation does not involve NCO 47. In fact, NCO 47 does not have shown any modulating input. The principle of operation there is entirely different. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

5) Claims 8, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) and Kim et al. (U.S. Patent No. 2002/0034260), as

applied to claims 7 and 15 above, and further in view of Park et al. (U.S. Patent No. 6,373,902). Applicants respectfully traverse this rejection, as set forth below.

Claim 8 further defines the circuit of claim 7, the phase modulated path comprising a gain normalization component that adjusts the second digital input for process, voltage and temperature (PVT) variations associated with the digitally controlled oscillator. Examiner admits that Ahn and Kim fail to disclose the phase modulated path comprising a gain normalization component that adjusts the second digital input for PVT variations associated with the oscillator. Examiner, however, relies upon Park for such teaching. Applicants respectfully point out that even if, arguendo, Park were to disclose what Examiner suggests, Park fails to teach or the previously described deficiencies of a combination of Ahn and Kim as applied to Claim 7 above. Applicants further rely upon their responses above in support of the allowance of Claims 2 and 22. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 16 further defines the circuit of claim 15, the phase modulated path comprising a gain normalization component that adjusts the second digital input for process, voltage and temperature (PVT) variations associated with the digitally controlled oscillator. Examiner admits that Ahn and Kim fail to disclose the phase modulated path comprising a gain normalization component that adjusts the second digital input for PVT variations associated with the oscillator. Examiner, however, relies upon Park for such teaching. Applicants respectfully point out that even if, arguendo, Park were to disclose what Examiner suggests, Park fails to teach or the previously described deficiencies of a combination of Ahn and Kim as applied to Claim 15 above. Applicants further rely upon their responses above in support of the allowance of Claims 2 and 22. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 19 further defines the circuit of claim 14, the amplitude modulated path comprising a gain normalization component that adjusts the first digital input for process, voltage and temperature (PVT) variations associated with the digitally controlled oscillator. Examiner admits that Ahn and Kim fail to disclose the phase modulated path comprising a gain

normalization component that adjusts the second digital input for PVT variations associated with the oscillator. Examiner, however, relies upon Park for such teaching. Applicants respectfully point out that even if, arguendo, Park were to disclose what Examiner suggests, Park fails to teach or the previously described deficiencies of a combination of Ahn and Kim as applied to Claim 14 above. Applicants further rely upon their responses above in support of the allowance of Claims 2 and 22. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

6) Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Pub. No. 2002/0080891) in view of Park et al. (U.S. Patent No. 6,373,902). Applicants respectfully traverse this rejection, as set forth below.

Claim 24 requires and positively recites, an integrated transceiver circuit, comprising: "means for producing a digital input", "means for predistorting the digital input to mitigate nonlinear error associated with a power amplifier according to one or more predistortion parameters", "means **for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain**", "means for generating an analog signal from the digital input" and "means for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting".

Examiner admits that Ahn fails to disclose means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain. Examiner, however, relies for Park for this omitted teaching. Applicants respectfully traverse Examiner's determination for the reasons set forth below.

Ahn in view of Park does not teach "means **for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain**", as required and positively recited by Claim 24. The text cited by the examiner (Park, col. 3, lines 35-57) merely discloses a function "to update digital codes stored in a predistortion random-access-memory (RAM) 21 in a direction such as to reduce the distortion" (Park, col. 3, lines 55-

57). The cited text only loosely deals with voltage compensation – NOT gain normalization. These two are different. There is no gain normalization component in Park as is conventionally understood and described in the present disclosure. For example, the "phase information associated with the normalized tuning word is normalized to an expected clock period of oscillator" (pp. 4, lines 19-20), which is not taught by Park. Further, "The IPA gain normalization component 124 operates in much the same fashion as the DCO gain normalization device. The exact gain provided by the power amplifier for a particular input is subject to process and environmental factors which cannot be known precisely, so an estimate thereof, K'_{IPA}, must be determined. The estimate K'_{IPA} can be calculated entirely in the digital domain by observing responses to past gain corrections. The actual IPA gain estimation may involve arithmetic operations, such as multiplication or division and averaging, or an exhaustive or iterative search for an optimal solution..." (pp. 10, lines 16-23). Accordingly, the estimation of the PA gain is not taught by Park. Therefore, Park fails to teach or suggest, means **for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain,** as required by Claim 24. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 25 further defines the circuit of claim 24, the means for generating the analog signal comprising means for synthesizing a radio frequency signal from a digital input. Claim 25 stand allowable for the reasons set forth above in support of the allowability of Claim 24. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claim 26 further defines the circuit of claim 24, the means for analyzing the analog signal including means for applying a direct current (DC) offset to the signal. Claim 26 stand allowable for the reasons set forth above in support of the allowability of Claim 24. Moreover, Ahn does not teach, suggest or provide motivation for adding a DC offset to the signal, which is described in our patent application as "DC offset is provided to the signal to mitigate a strong in-channel DC component of the signal. The specifics of the conditioning will depend upon the characteristics of the signal." (pp. 20, lines 22-25). The cited text by the Examiner (Ahn [0041])

does not discuss it. Accordingly, the 35 U.S.C. 103(a) rejection is overcome.

Claims 1-26 stand allowable for the reasons set forth above. New Claims 27-32 similarly stand allowable. Applicants respectfully request withdrawal of the remaining rejections and allowance of the application at the earliest possible date.

Respectfully submitted,

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